“Research is to see what everyone else has seen and think what no one else has thought.”

— Albert Einstein
Integrated Circuit
Outlier Identification by
Multiple Parameter Correlation

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Outline

- Introduction
- Problem Definition
- Prior Work
- Research Goals
- Research Plan
- Summary
Test: Needle Search In Haystack

Intel® Pentium 4 chip layout

130 nm technology
Miles of copper interconnect
42 million transistors

© Intel Corporation
Smaller Needle, Bigger Haystack
Semiconductor Economics 101

- **Cost – the prime drive for technology**
  - Manufacturing cost/transistor falls rapidly
    - higher performance/cost ratio
  - Complexity increasing with each technology advancement
    - Test cost falls slowly
    - Increasing test cost contribution to overall cost

- **Tester time extremely valuable**
  - Important to find defective chip early in test cycle or manufacturing flow
Basic Testing Methodology

Defect detected only if output different from fault-free output

Apply inputs to excite the defect
and propagate its effect to the output
So Many Defects, So Little Time

- Billions of possible defects
  - Fortunately have similar effect on electrical characteristics
- Modeled using higher level of abstraction called “fault”
  - Defect \(\rightarrow\) physical (e.g. short between lines)
  - Fault \(\rightarrow\) electrical (e.g. increased current)
- Many (possible) defects map to the same fault
IC Testing Methods

- Functional testing (Black box)
  - Verify “correctness” of chip, conformance to specifications
  - Exponential test time

- Structural testing (White box)
  - Verify “integrity” of chip structure
  - Too abstract, no implicit confidence about function

- Defect-based testing
  - Verify absence of defect
  - If no defects detected, chip should be fault-free

- Test methods complementary in nature
Defect-based Test Types

- **Boolean test**
  - Can distinguish between faulty or fault-free chips

- **Continuous parameter test**
  - No clear faulty/fault-free distinction
  - Leakage current ($I_{DDQ}$) test
Leakage Current ($I_{DDQ}$) Test

- Primary measurement leakage current
- Current drawn from the supply when the inputs are stable
- Can be measured at power supply ($V_{DD}$) line or at the ground (called $I_{SSQ}$)
Basics of $I_{\text{DDQ}}$ Testing

- Premise: Fault-free CMOS chips have low leakage

![Diagram of CMOS circuit with $V_{\text{DD}}$, Input, Output, and $I_{\text{DD}}$, $I_{\text{DDQ}}$ levels over time]
Defect Types

- Active (pattern-dependent) defect
  - Leakage current high for some but not all patterns
  - e.g. gate-to-source short, gate oxide short

- Passive (pattern-independent) defect
  - High leakage current for all input patterns
  - e.g. $V_{DD}$-GND short
Advantages of $I_{DDQ}$ Testing

- Simple, intuitive
- No propagation requirements
  - 100% observability
- Fortuitous detection
  - Fewer vectors needed for higher fault detection capability
- Detects several defect types
  - GOS, stuck-on, punch-through, bridges
- Detects some *latent* defects
  - Useful for screening low-reliability chips
Conventional $I_{DDQ}$ Testing

- Single threshold method
  - Threshold decided using circuit simulations or empirically
Technology Impact on $I_{DDQ}$ Test

- Reduced transistor geometries
  - Increases leakage current exponentially
  - Increased process variations
    - Cannot distinguish between faulty and fault-free leakage currents using a single threshold
- Small threshold rejects too many good chips
  - Yield loss (lost revenue)
- High threshold accepts too many flawed chips
  - Test escapes (customer returns)
## ITRS Projections for $I_{DDQ}$

<table>
<thead>
<tr>
<th>Year</th>
<th>Gate Length (nm)</th>
<th>$I_{DDQ}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2001</td>
<td>90</td>
<td>30 – 70 mA</td>
</tr>
<tr>
<td>2003</td>
<td>65</td>
<td>70 – 150 mA</td>
</tr>
<tr>
<td>2005</td>
<td>45</td>
<td>150 – 400 mA</td>
</tr>
<tr>
<td>2008</td>
<td>35</td>
<td>400 mA – 1.6A</td>
</tr>
<tr>
<td>2011</td>
<td>25</td>
<td>1.6 – 8 A</td>
</tr>
<tr>
<td>2014</td>
<td>15</td>
<td>8 – 20 A</td>
</tr>
</tbody>
</table>

For high-performance microprocessor circuits

$I_{DDQ}$ Test in Deep Sub-Micron

Earlier Technologies

Deep Sub-Micron Technologies

Fault-free

Faulty

Threshold

.user_comment:

Test Escapes

Yield Loss

$I_{DDQ}$

$I_{DDQ}$
$I_{DDQ}$ and Defect Severity

- Fault-free
- Subtle defect
- Gross defect
- Fatally flawed
$I_{DDQ}$ Too Important to Lose

- Important component of test suite
  - Capable of detecting some unique defects
  - When used with other test methods, it can reduce test escapes/defect level
- Detects some *latent* defects
  - Useful for screening low reliability chips
  - Useful as an alternative to burn-in (BI)
  - BI less effective and expensive for DSM technologies
    - Reduced voltage and temperature acceleration
I\textsubscript{DDQ} Only a Part of the Puzzle

- Increased Leakage
- Inaccurate Fault models & New Defect Mechanisms
- Increased Test cost
- Process Variability
- Test time/data Reduction & Insufficient Fault coverage
- Reliability Screens losing effectiveness
Research Focus

This research focuses on using statistical outlier rejection methods for identifying flawed chips that might lead to functional failure.
Why Use Outlier Detection?

- Continuous parameter spectrum
  - Must distinguish flawed chips from “fatally” flawed ones
- Flawed chips show different behavior than others
  - Appear as an “outliers”
  - Outlier detection useful for differentiation
What is an Outlier?

- Outlier
  - A chip that exhibits markedly different parameter(s) or variation in parameter(s) compared to other chips
- Improving confidence in differentiating “true” outliers is the motivation for this research
Outlier Identification Methods

- Reliance on properties of standard distributions
  - Mean, standard deviation, median, range

- Various methods
  - Z-scores test
  - Chauvenet’s criterion
  - Tukey method
  - Median of Absolute Deviations (MAD) test
Why is Outlier Detection Difficult?

- Outliers affect properties of the distribution
- Several orders of magnitude variation in fault-free $I_{DDQ}$ itself
  - Makes difficult to distinguish between a “true” outlier and an “apparent” outlier
- Outliers chips are functionally okay
  - Manufacturer’s dilemma (yield loss vs. quality)
No Silver Bullet

Wafer level data for a vector

- N = 179
  - Mean 19.58 µA
  - STD 176.35

- N = 176
  - Mean 2.5 µA
  - STD 8.3

- N = 166
  - Mean 0.84 µA
  - STD 1.43

- N = 151
  - Mean 0.44 µA
  - STD 0.18

- N = 197
  - Mean 678 µA
  - STD 2142.65
Suggested Solution Methods

- **Approach 1**
  - Reduce fault-free $I_{DDQ}$
    - Makes identifying faulty $I_{DDQ}$ easier

- **Approach 2**
  - Estimate fault-free $I_{DDQ}$ accurately

- **Approach 3**
  - Reduce variation in fault-free $I_{DDQ}$ data
    - Makes faulty $I_{DDQ}$ “stand out”
  - Category known as $I_{DDX}$
Approach 1: Reducing Fault-free $I_{DDQ}$

- Reduce temperature
  - Too expensive, slow, impractical
  - Less effective for future technologies
- Reverse (back) body bias
  - Technology change, inflexible
  - Less effective due to limited backbias voltage
- Silicon-On-Insulator (SOI)
  - Different technology, learning curve
- Multiple-threshold transistors
  - Performance tradeoff, less effective in future
Approach 2: Estimating Fault-free $I_{DDQ}$

- Model-based estimation
  - Usually switch-level (transistor) modeling
  - Mostly design-specific
  - Time consuming for large chips
  - Does not address process variation issue very well
- Empirical estimation of fault-free $I_{DDQ}$
  - Requires extensive analysis of data
Die 1 $I_{DDQ}$ Variation
Die 2 $I_{DDQ}$ Variation

Small spread
Die 1 and Die 2 $I_{DDQ}$ Variation

[Graph showing the comparison of $I_{DDQ}$ readings for Die 1 and Die 2]
Die 1, 2 and 3 $I_{DDQ}$ Variation

Is Die 1 really Defective?
Difficult to determine which of these dice are Defective and which ones are fault-free.
Approach 3: 
$I_{DDX}$ Test Methods

- Current Signature
- Delta-$I_{DDQ}$
  - Histogram-based Method
- Correlation with other parameters
  - Wafer XY location
  - Frequency ($F_{max}$)
  - Flush delay
Current Signature [Gattiker, Maly]

- Signature – sorted $I_{DDQ}$ measurements
- A chip with active defect shows a “step” or “jump” in the signature
  - Indicates multiple paths current can take
- Fault-free chip shows smooth signature
  - Also true for passive defects
  - Cannot screen passive and subtle active defects
Current Signatures Example

- Passive Defect?
- Active Defect
- Faulty/Fault-free?
- Fault-free

Graph showing IDDQ in μA over vector number.
Differential/Delta $I_{DDQ}$ [Thibeault]

- Differences (deltas) in consecutive readings small for a fault-free chip
- Background leakage gets cancelled
  - Cannot screen passive defects
- Less effectiveness in future [Krusemann]
Histogram-based Analysis

Reduce $\sigma$, Mean $\sim 0$
Current Ratios [Maxwell et al.]

- CR relatively constant for fault-free chips
  \[
  CR = \frac{\text{Max } I_{DDQ}}{\text{Min } I_{DDQ}}
  \]
- Measure $I_{DDQ}$ for the "minimum $I_{DDQ}$ vector"
  - Set limits on all other vectors dynamically
  - Min. $I_{DDQ}$ vector changes from chip to chip
Current Ratios Example

![Graph showing current ratios with labels: lower current die (left axis, smoothed) and high current die (right axis).]
Threshold Selection Challenge

Which is the “correct” threshold?

\[ I_{DDQ} > 5 \, \mu A \]
\[ I_{DDQ} < 5 \, \mu A \]
Outlier Identification by Correlation

- Correlation useful for estimating fault-free $I_{\text{DDQ}}$
  - Can be used for outlier identification
- Different methods
  - Vector-to-vector correlation [Unni et al.]
  - Die-to-die correlation
  - Die XY position on wafer [Daasch et al.]
  - Other parameters
    - $F_{\text{max}}$ [Keshavarzi et al.]
    - Flush delay [Sabade et al.]
Motivation: Spatial Correlation

- Similar process conditions for neighboring chips on a wafer
- Fault-free chip parameters are expected to be similar
- A sudden change in any parameter is indicative of anomalous behavior
  - Likely defective [Singh et al.]
  - Called “spatial outliers”
Spatial Outlier Example

Spatial outliers

IDDQ (µA)

Y Coordinate

X Coordinate
Local Neighborhood Definition

Center die
Estimation of Fault-free $I_{DDQ}$

- Use neighboring chips’ $I_{DDQ}$ for estimating fault-free $I_{DDQ}$ of the center die
  - If actual $I_{DDQ}$ is higher, center die is likely to be defective
  - If actual $I_{DDQ}$ is lower, neighbor die could be defective
- How high is high? How low is low?
  - Threshold setting does not disappear
Correlation Methods

- Spatial/plane fit
- Neighbor Current Ratios (NCR)
- Immediate Neighbor Difference $I_{DDQ}$ Test (INDIT)
- Correlation with flush delay
Plane Fit

- $I_{DDQ}$ function of neighboring dice $I_{DDQ}$ and die’s XY position on wafer
  - First reject gross outliers
  - Linear regression
- $Z (I_{DDQ}) = A \cdot x + B \cdot y + C$
Neighbor Current Ratios (NCR)

- Two neighboring chips should have similar $I_{DDQ}$ for identical vectors $i$

\[
NCR (i) = \frac{I_{DDQ \text{ die 1} (i)}}{I_{DDQ \text{ die 2} (i)}} \sim 1
\]

- Process variations cause NCRs to vary
  - Mean value close to 1
- High NCR indicates defective die (Die 1)
NCR Illustration

Obvious spatial outliers
Healer Chips and CR/NCR

- Healer – a chip that shows elevated $I_{DDQ}$ before BI and reduced $I_{DDQ}$ after BI
- Need more careful analysis

![Graph showing correlation between CR and Max NCR]
Immediate Neighbor Difference

$\text{IND}_\text{DDQ}$ Test (INDIT)

- Ratios may pass some outliers
- Differences in $I_{\text{DDQ}}$ for same vectors $\sim 0$
  - Process variations cause variation

\[
\text{IND} (i) = I_{\text{DDQ} \text{ Die 1} (i)} - I_{\text{DDQ} \text{ Die 2} (i)} \sim 0
\]
Why Multi-parameter Test?

- $I_{\text{DDQ}}$ test alone not enough
  - Pass/fail decision difficult and prone to error
  - Can result in yield loss/test escapes
- Need higher confidence in detecting flawed chips
- Defect detection capability diminishing for each test method in isolation
  - Defect detection harder with each technology node
$I_{DDQ}$ & Flush Delay Correlation
Research Goals

- Identify outlier chips
  - Distinguish between real and seemingly outliers
- Exploit wafer-level spatial dependence
- Correlate multiple test measurements
  - Vector-to-vector for the same chip
  - Across multiple chips, wafers or lots
- Evaluate possibility for burn-in reduction
Research Plan - I

- Extensive analysis of SEMATECH data
  - Evaluate different ideas
  - Correlate with BI results to validate methods
  - Data rather outdated (0.6 micron)
- Recent data obtained from LSI Logic
  - No BI data available
  - How to validate methods?
- Proposal sent to Texas Instruments
- Discussed with Philips, IBM, Sony
Research Plan - II

- Use advanced statistical methods
  - Factor analysis
  - Understand underlying process variations, compare estimated $I_{DDQ}$ with model
- Evaluate different outlier identification methods
  - Chauvenet’s criterion, Tukey method, Median of Absolute Deviations (MAD), etc.
  - Evaluate use of mean vs. median
- Estimate yield loss/defect level improvements
Research Contributions

- Systematic identification of outlier chips
- Neighboring chips’ parameter-based estimation and statistical analysis for defective chip screening
- Insight into underlying process variations
- Possible burn-in reduction or elimination
  - Test cost reduction
Research Benefits

- Early detection of defective chips or latent defects
- Understanding process glitches, variations & yield excursions
- Burn-in reduction or elimination
- Test cost reduction, Reduced DPM
- Reduced customer returns
- Increased Profit
Summary

- Defect-based VLSI testing faces difficult challenges; $I_{DDQ}$ test loses its effectiveness
- Single parameter testing loses its effectiveness in screening faulty chips
- Correlating multiple test measurements necessary to screen true outliers
- Wafer-level test can be useful in reducing test time and overall test cost
  - Has potential to reduce burn-in
Questions?
Backup Slides
Pattern Dependent Defect

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th>IDDQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>low</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>high</td>
</tr>
</tbody>
</table>

Defect Detected!

Gate to source short
Pattern Independent Defect

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<th>Output</th>
<th>IDDQ</th>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>high</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>high</td>
</tr>
</tbody>
</table>

Resistive bridge
Short Channel Effect

Gate begins to lose Control over the channel Effective $V_{th}$ reduced ($V_t$ Roll-off)
Process Variation Levels

Frequency

Parameter Value

Lot to lot
Wafer to wafer
Inter die (same wafer)
Intra-die (vector)
VLSI Technology Advancement

- Reduced transistor geometries
  - Higher transistor counts
- Higher levels of integration (SoC designs)
- Increasing device complexity (9 metal layers)
- Mixed signal design (more analog)
- New materials (low-K, high-K)
- Lower supply and threshold voltages
- Higher leakage currents and power dissipation
Technology Impact on Testing

- Reduced transistor geometries
  - Increased process variations
- New defect mechanisms
  - Inaccurate fault models
- Higher levels of integration
  - Reduced observability and controllability of defects
- Higher leakage currents
  - Unable to distinguish faulty currents
- Reduced voltage, increased temperature
  - Reduced effectiveness of reliability screens
Impact on $I_{DDQ}$ Testing

- Reduced transistor geometries
  - Reduced supply voltages to avoid gate oxide breakdown
  - Necessary to reduce threshold voltage for performance requirements
  - Increases leakage current exponentially
- Cannot distinguish between faulty and fault-free leakage currents using a single threshold
  - Unacceptable yield loss and/or test escapes
- Large process variations make it worse!
Scaling Implications on IOFF

ITRS Projections for High-performance Microprocessors

- **35 nm Node**: $L_G = 22$ nm, $t_{ox} = 5.5$ Å
- **50 nm Node**: $L_G = 32$ nm, $t_{ox} = 7$ Å
- **70 nm Node**: $L_G = 45$ nm, $t_{ox} = 10$ Å
- **100 nm Node**: $L_G = 65$ nm, $t_{ox} = 13$ Å
- **130 nm Node**: $L_G = 85$ nm, $t_{ox} = 17$ Å
- **180 nm Node**: $L_G = 140$ nm, $t_{ox} = 25$ Å

Target Supply Voltage ($V_{DD}$)

$I_{ON}$ (NMOS) = 750 µA/µm
$I_{ON}$ (PMOS) = 350 µA/µm

(independent of supply voltage)
CMOS Scaling Fundamentals

Scaling to $1/K$ reduces the drain current $I_d = W/L \cdot V^2/\text{Tox}$.

Propagation delay is reduced to $1/K$. 
Non-uniform Scaling Trends

- $T_{ox}$ scales faster than $V_{DD}$
- Increased electrical field
- Performance depends on $V_{DD} - V_t$
- $V_t$ scales slower than $V_{DD}$ due to Boltzmann statistics

Source: ITRS 2001
$I_{DDQ}$ Variation (All Chips)

“All pass” chips
“All Pass” Chips $I_{DDQ}$ Variation

Several outliers
Are all defective?
Actual $I_{DDQ}$ Distribution

Optimum Threshold?
Leakage Current Components

Reverse biased PN junction leakage
Subthreshold current (weak inversion)
Gate Induced Drain Leakage (GI DL)
**Drain Induced Barrier Lowering (DIBL)**
  Punch-through Leakage
Tunneling leakage through gate oxide
Leakage Current Components

- Reverse biased PN-junction leakage
- Gate Induced Drain Leakage (GIDL)
- Tunneling leakage
- Subthreshold leakage
- Drain Induced Barrier Lowering (DIBL)
- Punch-through leakage

Input = 0

Output = 1
Major $I_{DDQ}$ Components

- GIDL
- Weak inversion & Junction leakage
- DIBL

Graph with $V_D$ values of 4.0 V, 2.7 V, and 0.1 V.
“Automatic Test Equipment (ATE) is a misnomer. It should be called Automatic Measuring Equipment (AME). ... We need statistical methods to discriminate faulty chips [from fault-free ones].”

- Robert Madge (LSI Logic) at *Industrial Test Challenges* talk at Intel in May 2002
Two Signature Types

Pattern Dependent Current Signature

Pattern Independent Current Signature (Background leakage)
Radial $I_{DDQ}$ Variation

$I_{DDQ}$ for a single vector shown
Handling Defect Clustering

Scratch
226 defects,
Mechanical handling

Defects detected with
Optical in-line tools

Particle contamination
617 defects,
CVD process contamination

Source: Semiconductor Spatial Signature Analysis (SSA)
Correlation: What Does It Mean?

- Positive correlation
- Negative correlation
- No correlation
Why $I_{DDQ}$ Correlates to Delay?

- Smaller $L_{eff} \rightarrow$ faster transistor
- Smaller $L_{eff} \rightarrow$ more leakage

![Diagram showing the relationship between $L_{eff}$ and transistor properties](image)
How Reverse Body Bias Works?

- Reverse potential applied to substrate increases effective $V_{th}$
- This reduces leakage current
- Penalty $\rightarrow$ switching speed reduces
### All Tests Are Needed

Distribution of package test results for SEMATECH data

<table>
<thead>
<tr>
<th></th>
<th>5 uA IDDQ Test</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>P</td>
<td>P</td>
<td>F</td>
</tr>
<tr>
<td>P</td>
<td>6</td>
<td>1463</td>
<td>7</td>
</tr>
<tr>
<td>P</td>
<td>14</td>
<td>0</td>
<td>34</td>
</tr>
<tr>
<td>F</td>
<td>6</td>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td>F</td>
<td>52</td>
<td>36</td>
<td>1251</td>
</tr>
</tbody>
</table>

- **Stuck-at Test**
- **Delay Test**
- **Functional Test**

P – Pass, F – Fail
Is $I_{DDQ}$ Irreplaceable?

150000 die at wafer, 76000 dice after package, package values normalized to wafer good parts
Source: Peter Maxwell, Talk at Industrial Test Challenges, May 2002.
Fewer Vectors, Higher Coverage

For same FC I_{DDQ} tests require many fewer vectors than functional test
Optimum Threshold Selection

- **Cost vs. Quality debate**

  - **Zero Test Escapes**
  - **Optimum Threshold**
  - **Zero Yield Loss**

  - High Overkill
  - High Defect Level

- **Frequency**

  - Fault-free chips
  - Faulty chips

- **$I_{DDQ}$**
Wafer-level Analysis: Advantages

- Detection of defective chips at wafer probe
  - Reduction in test costs and time
  - Reduced packaging cost/die
- Provides insight into understanding underlying process variations
  - Useful for detecting process glitches
- Different pass/fail criterion for different wafers
  - Reduce yield penalty for fast and leaky wafers
Values on Logarithmic Scale

![Graph showing values on a logarithmic scale with vector number on the x-axis and IDDQ in uA on the y-axis. The graph includes multiple lines representing different DIE samples (DIE_1, DIE_2, DIE_3, DIE_4).]
Delta $I_{DDQ}$ Illustration

First measurement

$I_{DDQ}$

Defective

Defective

Guard band

Vector number
Defect Detection

Source: icknowledge.com
Technology Trends
\( I_{DDQ} \) Test for Deep Sub-Micron

- Yield loss and test escapes inevitable

[Diagram showing frequency distribution of fault-free and faulty chips for Earlier Technologies and DSM Technologies, with \( I_{DDQ} \) and \( I_{th} \) indicated.]