“Research is the simple pleasure of discovering something that you didn’t know before.”

- Carl Friedrich Freiherr von Weizsacker
I'm not an outlier; I just haven't found my distribution yet.
A Tale of Two Chips: A Dilemma

Chip A
Leakage: 1 mA

Chip B
Leakage: 100 mA

Is chip ‘B’ simply *different* or defective?
Ship or reject?

Is your answer the same if there are 1 million of each type?

This talk will review some strategies to solve this problem
Outline

- VLSI Testing
- Dilemma of Parametric Tests
- Review of Prior Work
- Proposed Approaches
- Analyses of Industrial Data
  - IBM, LSI and TI Data
- Conclusions
- Future Work
Outline

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Technology Trends

• Transistors are getting smaller
  – 130 nm in production, 90 nm in progress

• Manufacturing cost/transistor falls
  – More functions for same cost
  – More complex, bigger, faster chips
    • AMD Athlon® - 55 million transistors
    • Pentium 4® - 77 million transistors

• Higher reliability requirements
  – Failures are expensive → testing is inevitable
Typical IC Test Flow

- **Manufacturing**
  - Wafer
  - Wafer Probe Test
  - Test (Pass/Fail)

- **Assembly and Test**
  - Package Test
  - Accepted chips
  - Rejected chips

- **Stress Test (Burn-in)**
  - BI pass
  - BI fail

- **Post-BI Test**

**Test cost increases 10x with each level**

- $0.01 (Wafer)
- $0.1 (Test)
- $1 (Package)
- $10 (Stress Test)
- $100 (System)

**Customer return**
Test – an Imperfect Screen

- Good chips
- Bad chips

Reject

Test

Accept

Overkill (yield loss)

Test escape (defect level)
VLSI Test: A 1-min Crash Course

IDDQ test

Apply inputs to excite the defect

Propagate its effect to the output

defect is detected only if faulty output differs from fault-free output
VLSI Test Classification

- **Functional**
  - Check functionality
  - More test generation effort
  - Exponential with number of inputs

- **Structural**
  - Check structure e.g. stuck-at test

- **Defect-based**
  - Assume defect model
  - Compare good and fault-free chip behavior

- **Parametric**
  - Parameter within limit
  - No device specification

Test methods are complementary
IDDQ Testing: Basics

- Premise: fault-free chips have low leakage (no conduction path from VDD to GND)
Conventional IDDQ Testing

- Single threshold method
  - Threshold decided using circuit simulations or empirically

![Diagram showing Accepted and Rejected chips based on IDDQ and Threshold]
### IDDQ Values for DSM Chips

For high-performance microprocessor circuits  

<table>
<thead>
<tr>
<th>Year</th>
<th>Gate Length (nm)</th>
<th>IDDQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>2001</td>
<td>90</td>
<td>30 – 70 mA</td>
</tr>
<tr>
<td>2003</td>
<td>65</td>
<td>70 – 150 mA</td>
</tr>
<tr>
<td>2005</td>
<td>45</td>
<td>150 – 400 mA</td>
</tr>
<tr>
<td>2008</td>
<td>35</td>
<td>400 mA – 1.6A</td>
</tr>
<tr>
<td>2011</td>
<td>25</td>
<td>1.6 – 8 A</td>
</tr>
<tr>
<td>2014</td>
<td>15</td>
<td>8 – 20 A</td>
</tr>
</tbody>
</table>
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Pass/Fail Limit Setting Challenge

- Long tailed distribution
- Too low threshold
  - yield loss
- Too high threshold
  - defect level

Are these chips outliers or 'normal' process variations?
Dilemma of Parametric Tests

• Chips are functional
  – Reluctance to discard unless proved defective
    • innocent until proved guilty

• No clear faulty/fault-free distinction
  – No specification; long tail

• Even 1-2% yield loss can mean million$
  – Quality vs. revenue issue
What is an Outlier?

- **Outlier**
  - A chip that exhibits markedly different parameter(s) or variation in parameter(s) compared to other chips
  - We use IDDQ and delay test data
- Improving confidence in differentiating “true” outliers (defective chips) is the motivation for this research
Why Outlier Detection?

• Being indifferent to anomalous behavior is not affordable
• Outliers have poor reliability
  – Affect outgoing quality
  – Can result in costly customer returns
• Pass/fail threshold setting difficult
  – Customer returns vs. returning customers
Outlier Detection Difficulty

Not so easy when gray sheep exist

Easy to spot a black sheep
Outliers: Subtle, Marginal, Hidden

Today’s Test challenge: finding a specific zebra
Research Goals

• Identify outlier using wafer-level parametric test data
  – Exploit wafer-level spatial correlation
    • Correlate multiple parameters
    • Compare effectiveness of methods
    • Data from IBM, LSI Logic, Texas Instruments
      – Primarily IDDQ test data, also delay data
  – Not inventing outlier detection methods; but improving outlier screening capability
Why is Outlier Detection Difficult?

• **Outlier definition depends on distribution**
  – Outliers affect properties of distribution
  – Chicken and egg problem

• **Several orders of magnitude variation in fault-free parameter itself (e.g. IDDQ)**
  – Makes difficult to distinguish between a “true” outlier and an “apparent” outlier

• **Methods assume standard distribution**
  – Data transformation hard to find

• **Outlier chips are functionally okay**
  – Manufacturer’s dilemma (yield loss vs. quality)
IDDQ Distribution: Reality

Thresholds are arbitrary

IBM data single wafer
No Silver Bullet Threshold
Outlier Rejection Methods

- Many flavors
  - Z-scores test
  - Chauvenet’s criterion
  - Tukey method
  - Median of Absolute Deviations (MAD) test
- Rely on properties of standard distributions
  - Mean, standard deviation, median, range
- Need resistant estimation
How to Detect Outliers?

• **Outliers**
  – something that is situated away from or classed differently from a main body [Merriam-Webster]

• **Define “normal” or “main” body**
  – Simulation/model building
    • Usually design-specific, time consuming
    • Difficult to account for all variations
  – Empirical analysis
    • Data driven strategy (characterize data)
    • Analysis as good as learning sample of data
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Prior Work

• **Statistical post-processing of wafer test data**
  – Goal: variance reduction of fault-free IDDQ data
  – Within-chip IDDQ variation
    • Current Signature [Gattiker & Maly]
    • Delta-\(I_{DDQ}\) [Thibeault]
    • Current Ratio [Maxwell et al.]
  – Within-wafer IDDQ variation
    • Nearest Neighborhood Residual (NNR) [Daasch et al.]
Current Signature*

• Sort all IDDQ measurements
• A chip with active defect shows a “step” or “jump” in the signature
  – Indicates multiple paths for IDDQ
• Fault-free chip shows smooth signature
  – Also true for passive defects
    • Cannot screen passive/subtle defects
• Pass/fail threshold for step size
  – Use statistics combined with empirical analysis

[*Gattiker and Maly, ITC 1997*]
Current Signature Example

- Passive defect
- Active defect
- Faulty/Fault-free?
- Fault-free
Delta IDDQ*

- Take differences (deltas) in consecutive readings
  - Small for a fault-free chip
  - Background leakage gets cancelled
- Easy production implementation
- Cannot screen passive defects
- Ineffective at about 100 mA [Kruseman, ITC 2001]

[* Thibeault, ITC 1999]
\( \Delta \text{IDDQ Example} \)

Defective \( \Delta \text{IDDQ} \) clusters

Fault-free

Faulty

Passive defect
Current Ratio*

- Ratio of max to min IDDQ of a chip
  - Relatively constant for fault-free chips
- Ease of production implementation
- Measure IDDQ for all vectors, find CR
  - If CR > threshold, reject the chip
- Difficult to screen passive defects
- CR threshold setting challenge

[*Maxwell et al., ITC 1999*]
Current Ratio Example

![Graph showing current ratio example]
CR Threshold Selection

Outliers

Slope = CR

12128 chips
Limitations of CS, CR and $\Delta$IDDQ

- Consider only within-chip variance
- Ineffective way to screening outliers
  - CR for 20 $\mu$A within-chip variance
    - 4-24 $\mu$A $\rightarrow$ CR = 6
    - 20-40 $\mu$A $\rightarrow$ CR = 2
    - 100-120 $\mu$A $\rightarrow$ CR = 1.2
  - Low CR does not imply a fault-free chip
  - Difficult to screen passive defects
    - Reliability hazards [Agilent Technologies study]
Nearest Neighbor Residual*

- Estimate IDDQ using neighboring die IDDQ
  - Consider correlated neighbors
  - Use median IDDQ as an estimate

[*Daasch et al., ITC 00*]
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Proposed Approaches

• **Within-wafer IDDQ methods**
  – Wafer Signature*
  – Spatial Fit*
  – Neighbor Current Ratios (NCR)*
  – Immediate Neighbor Difference IDDQ Test (INDIT)*

[* Sabade & Walker]
Wafer-level Spatial Methods

- Similar process changes
  - Implies similar fault-free parameters
  - Deviation from “normal” variation is most likely due to defect
- Use neighboring die information to estimate permissible variation
  - Empirical model-building
- Accuracy subject to data used
  - Neighbors bias the model
Local Neighborhood Definition

Wafer

Center die
Spatial Outlier Example
Wafer Signature*

- Sort IDDQ readings for a vector for all chips on a wafer
  - Fault-free IDDQ same for good chips
  - Undergo similar process fluctuations
- Ideally smooth signature
  - Outliers in the “tail” of the signature
- A “break” in signature
  - Outliers or missing data?
- Threshold setting issue remains

[*Sabade & Walker, ITC 01, DBT 03]
Wafer Signature: Example

IDDQ (µA)

Chip number

Head

Tail

Breaks

Missing data
Spatial Fit Method*

• Use die \((x,y)\) coordinates and IDDQ as the z coordinate
• Linear regression
• \(Z = Ax + By + C\)
• Reject gross outliers

[*Sabade & Walker, ITC 2001]
Spatial Fit Illustration

Actual IDDQ  Estimated IDDQ  Residual IDDQ
Neighbor Current Ratios (NCR)*

- Two neighboring chips should have similar IDDQ for identical vectors $i$

\[
\text{NCR} (i) = \frac{I_{\text{DDQ die 1}} (i)}{I_{\text{DDQ die 2}} (i)} \sim 1
\]

- Process variations cause NCRs to vary
  - Mean NCR close to 1
- High NCR indicates die 1 is outlier

[*Sabade & Walker, DFTS 2002]
Neighbor Current Ratio (NCR)

\[ \text{NCR}(i) = \frac{I_{\text{DDQ}}(\text{chip1})(i)}{I_{\text{DDQ}}(\text{chip2})(i)} \]

- Chip 1 \(I_{\text{DDQ}}\) readings
- Chip 2 \(I_{\text{DDQ}}\) readings

\[ \text{NCR} = \max \{\text{NCR}(i)\} \]
\[ i = \{1 \ldots N*K\} \]
\[ N = \text{No. of neighbors} \]
\[ K = \text{No. of vectors} \]
NCR Illustration

“All-pass” chips from a wafer

Passive defect!

CR variation

NCR variation
NCR: Advantages & Limitations

• Advantages
  – Looks across wafer – better sensitivity
  – Scalable to future technology nodes
    • Fundamental variation mechanism remains same

• Limitations
  – Relative metric
  – Defect clustering reduces sensitivity
Immediate Neighbor Difference IDDQ Test (INDIT)*

- Differences in IDDQ for same vectors $\sim 0$
  - Process variations cause variation

$$IND (i) = I_{DDQ \ Die \ 1 \ (i)} - I_{DDQ \ Die \ 2 \ (i)} \sim 0$$

- Principle similar to NCR
  - Better screening capability than conventional delta-IDDQ
    - Considers within-neighborhood variability

[*Sabade & Walker, VLSI-Design 2003*]
Within-chip max. delta IDDQ

Within-neighbor max. delta IDDQ
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IBM (SEMATECH) Data

- Research experiment S-121, 1994-97
- 0.6 μm technology IC
- 18466 chips, 75 wafers
- Four tests conducted
  - Functional, stuck-at, delay, IDDQ
  - 5 μA threshold, 195 vectors IDDQ test
- Sample subjected to same tests
  - Pkg. Level, 6, 72 and 144 hrs burn-in
- Many chips fail only IDDQ test
  - Can be latent defects
LSI Data

- 180 nm technology IC, in production
- ~950000 chips, 1219 wafers
- 20 IDDQ vectors, ring osc. data
- Pass/fail thresholds confidential
- No burn-in data
  - Cannot conclusively determine “good” or “bad”
Spatial Fit Method Analysis Flow

- IDQ Data
- Normalize Transformation
- Gross Outlier Rejection
- Fault-free IDQ Estimation
- Inverse Transform

X
Y
wafer
Spatial Fit Method Details

• Used IBM/SEMATech data
  – Boolean fails ignored
  – Used 6-hr BI data for good/bad distinction
  – Analysis by ignoring/keeping IDDQ-only fail
Results (IDDQ-only fail=fail)

Chips

5 µA Threshold  Wafer median  Delta $I_{DDQ}$  Current Signature  Plane Fit

Rejected fail BI  Rejected pass BI  Accepted fail BI  Accepted pass BI
Results (IDDQ-only fail=pass)

![Bar chart showing the results of different parameters and thresholds for different categories: Rejected fail BI, Rejected pass BI, Accepted fail BI, and Accepted pass BI.](chart.png)
Spatial Fit Analysis

• Many IDDQ-only fail have smaller estimate
  – “true” spatial outliers easily identified
• Prior gross outlier removal necessary
  – Biases estimates, may keep outliers
• Wafer edge dice
  – Could not conclusively determine their fate
  – Can do selective burn-in
Why Multi-parameter Test?

- **IDDQ test alone not enough**
  - Pass/fail decision difficult and prone to error
  - Can result in yield loss/test escapes
- **Need higher confidence in detecting flawed chips**
- **Defect detection capability diminishing for each test method in isolation**
  - Defect detection harder with each technology node
Correlating Two Parameters

- **Vector-to-vector correlation**
  - Current Ratio
  - PCA-based analysis
- **Wafer-level methods**
  - Die (x,y) position and $I_{DDQ}$
- **Test parameters/metrics**
  - $I_{DDQ}$ and flush delay
  - CR and NCR
Flush Delay and $I_{DDQ}$

- Flush delay – measure of chip speed
  - Smaller $L_{eff} \rightarrow$ faster transistors
  - Smaller flush delay $\rightarrow$ more leakage
  - Average out across multiple transistors
- Use of test structures (e.g. RO)
  - Useful for early yield prediction (IBM)
- Correlation useful for identifying “marginal” outliers with higher confidence

[*Sabade & Walker, DBT 2002]
Illustration: IDDQ & Flush Delay

Smaller transistors switch faster and leak more
Useful for refining estimate obtained by spatial-fit method
Improved IDDQ Estimate

![Graph showing improved IDDQ estimate]

- **IDDQ (µA)**: Actual, spatial estimate, flush delay estimate, defective leakage

**Vector no.**

**IDDQ (µA)**

0 1 2 3 4 5 6 7

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49

**Flush delay estimate**

**Spatial estimate**

**Defective leakage**

**Actual**
CR/NCR Combination Insights

Region A
- Nominal CR
- Subtle active defects
- Spatial Outliers

Region B
- CR, NCR Outliers
- Active defects

Region D
- Nominal CR, NCR Outliers
- Fault-free Chips/
- Good chips in Bad neighborhood

Region C
- Outliers in Bad neighborhood

Passive defects
- in bad neighborhood

NCR Threshold
- Passive defects
IBM (SEMATECH) Data

- Passive defects
- Gross outlier tail
- All pass chips

Graph shows 605 chips, 606 chips, 60891 chips, and 26 chips.
Current Signatures (IBM data)
LSI Logic Test Data

Passive defects

Active defects

1041 chips

736 chips

Total 94,941 chips

93,972 chips

7,907 chips

CR inliers – defective?
Use of Additional Parameters

• **CROWNE**: Current Ratio Outliers With Neighbor Estimator
  – Using CR alone these chips are inliers
  – Outliers considering spatial neighborhood
  – Use NCR and further screening using additional parameter, say delay data

[*Sabade & Walker, DFTS 2003]
CR, NCR and Flush Delay

XY projection
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Conclusions

• Identifying outlier chips is critical
  – Poor reliability, cost, poor quality
  – Difficult for DSM technology chips

• Wafer-level spatial correlation useful
  – Applicable to future technologies as well

• More parameters needed to improve defect-screening resolution
  – Threshold setting issue remains

• Multivariate outlier rejection methods useful
  – Important to use proper transforms
Publications

1. ITC’01 – Improved Wafer-level Spatial Analysis for IDDQ Limit Setting
2. VLSI Des.’02 – Evaluation of Statistical Outlier Rejection Methods for IDDQ Limit Setting
3. VTS’02 – Evaluation of Effectiveness of Median of Absolute Deviations Outlier Rejection-based IDDQ Testing for Burn-in Reduction
4. DBT’02 – Wafer-level Spatial and Flush Delay Correlation Analysis for IDDQ Estimation
5. MWSCAS’02 – NCR: A Self-scaling, Self-calibrated Metric for IDDQ Outlier Identification
6. DFT ‘02 – Neighbor Current Ratio (NCR): A New Metric for IDDQ Data Analysis
7. VLSI Des.’03 – Immediate Neighbor Difference IDDQ Test (INDIT) for Outlier Identification
8. VTS’03 – Use of Multiple IDDQ Test Metrics for Outlier Identification
9. DBT’03 – Wafer Signature Analysis of IDDQ Test Data
10. DFT’03 – CROWNE: Current Ratio Outliers With Neighbor Estimator
11. VLSI Des.’04 – Comparison of Effectiveness of Current Ratio and Delta-IDDQ Tests
12. Design & Test Oct’02– IDDQ Test: Will It Survive the DSM Future?
13. Trans. on VLSI – Estimation of Fault-free IDDQ Using Wafer-level Spatial Information
14. JSA – IDDQ Data Analysis Using Neighbor Current Ratios

[All co-authored with D. M. H. Walker]
Contributions of This Work

• Investigated several outlier identification methods
  – Statistical methods
    • Chauvenet’s criterion, Tukey test, Median of Absolute Deviations (MAD) test, etc.
  – In general, no method is “perfect” solution
  – Underlying process must be known to use proper transformation
Contributions (Cont.)

- Exploited wafer-level spatial variation for outlier identification
  - Spatial-fit, NCR, INDIT, etc.
- Evaluated two metrics with DSM data
  - NCR and INDIT
    - More reliable than CR and delta-$I_{DDQ}$
    - No additional measurement needed
    - Applicable to future technologies
Contributions (Cont.)

• Evaluated *wafer signature* method
  – Combines best of current signature and delta-$I_{DDQ}$, useful for future technologies

• Proposed a new method for separating defect types detected by IDDQ test
  – CR-NCR combination is more powerful than CR alone
  – Combination verified using data from three technology chips
    • 0.6 µm, 180 nm and 130 nm
  – Useful for better outlier screening in future
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Scope of Future Work

• NCR, INDIT, etc. are relative metrics
  – Finding highly correlated neighbors
  – Wafer edge and fewer neighbor cases
• Using vector-to-vector correlation
  – Factor analysis-based model
  – Combine with other metrics like CR/NCR
  – Explore recent 130 nm data from TI
    • Effect of voltage-stress
Questions/Discussion

Thanks for your time!

Outlier (easy!)

Outlier (hidden)