Identifying defects in deep-submicron CMOS ICs

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Given the oft-cited difficulty of testing modern integrated circuits, the fact that CMOS ICs lend themselves to IDDQ testing is a piece of good fortune. But that valuable advantage is threatened by the rush of semiconductor technology to smaller feature sizes and faster, denser circuits, in line with the Semiconductor Industry Association's (SIA) Roadmap—its forecast for the CMOS IC industry. With safety margins for reliability, test, failure analysis, and design verification shrinking, it would be a shame to give up the IDDQ technique—and luckily, we may not have to. Steps can be taken to maintain its applicability as we rush deeper into the submicron regime. Before discussing them, however, a brief discussion of IDDQ testing seems to be in order. We will first examine why the IDDQ test serves several interests, then describe the challenge posed by 0.35-0.07-µm transistor geometries, and finally propose several solutions.

CMOS IC power supply current can be amperes during logic state transitions, but only nanoamperes during the steady state, or quiescent, portion of the clock cycle. This low quiescent power supply current, known as IDDQ, is what gives CMOS its traditional low-power edge over its technology competitors. But it does more than that. Engineers in design, fabrication, and test have learned to use this low quiescent current as a sensitive test to identify defects, which often prove to be the reason for customer returns, whether as test escapes or reliability failures. In fact, test escape levels below 200 parts per million have recently been attainable only by adding IDDQ testing. The technique has also eliminated the need for burn-in for some mature product lines. More, IDDQ measurements speed failure analysis by providing current-voltage signatures and temporal characteristics.

Detecting defects with current

Current is a more effective parameter than voltage for defect detection in CMOS ICs, although both are necessary for complete testing. The simple logic circuit with a bridging defect shown in Fig. 1 illustrates how IDDQ increases in the presence of a flaw. Bridging defects and certain open-circuit defects typically elevate the nanoampere levels of a normal circuit by two to seven orders of magnitude, providing very sensitive defect detection. If ICs are correctly designed and fabricated for low background current, then IDDQ is a relatively simple measurement with many benefits. But as background IDDQ rises, for whatever the reason, the effectiveness of IDDQ testing diminishes. For optimum detection of manufacturing defects, the defect-free IDDQ of an IC should be less than 1 µA.

Alan Righter and Dick Beegle, members of the technical staff of Sandia National Laboratories, Albuquerque, N.M., measured IDDQ on present-technology ICs and found the currents to be as given in the table. IDDQ generally increases with the active area of the IC.

<table>
<thead>
<tr>
<th>IDDQ measurements on CMOS ICs</th>
<th>Transistor count, thousands</th>
<th>Mean I_{DDQ}, nA</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. 1</td>
<td>70</td>
<td>0.4</td>
</tr>
<tr>
<td>No. 2</td>
<td>1500</td>
<td>320</td>
</tr>
<tr>
<td>No. 3</td>
<td>5000</td>
<td>980</td>
</tr>
</tbody>
</table>
Reliability and IDDQ

Defects cause reliability failures during a microelectronic product’s useful life. Whether a defect gives rise to a test failure at the factory or a product unreliability in a customer’s application depends mainly on the size and location of the defect in the circuit. Small mask-induced voids in metal lines may present the risk of failure due to electromigration, but a larger, open defect on the metal can cause an open circuit and a test yield failure. IDDQ is the most sensitive detection technique, and it can readily detect certain types of defects that affect yield and impact product reliability. Burn-in and life test data have both shown that IDDQ testing can reduce IC failure rates. Ken Wallquist, an engineer at Philips Semiconductors, Albuquerque, N.M., measured a 2.1-percent defect level associated with high IDDQ after a 24-hour burn-in experiment. Steve McEuen, an engineer at Ford Microelectronics, Dearborn, Mich., reported an 8.3-percent defect level for ICs with high IDDQ in a 1000-hour life test. Wallquist concluded that the elimination of burn-in for high-quality lots was economically justified when IDDQ testing was included. The reliability failure values depend heavily upon the IDDQ test level, IDDQ test vector coverage, and upon IC manufacturing quality. A defect can affect transistor operation by shifting the bias state into saturation. The saturated state sets up a high electric field in the drain region, which generates hot holes and electrons. Some of these hot carriers are injected into the transistor’s thin oxide, degrading switching time. Electromigration reliability risk for ICs occurs when the defect-induced high-IDDQ path includes narrow metal lines where the dense flux of electrons can move aluminum atoms of the conductor. Both open and bridging metal failures can result from electromigration. Modern metal lines typically have cross-sectional areas less than 0.25 µm² with correspondingly higher current densities than older IC technologies. The higher operating temperatures of complex, high-speed ICs also makes electromigration more likely to occur. IDDQ can to a significant extent screen out many of the defects that lead to a loss of reliability.

Failure analysis and IDDQ

When ICs are designed and fabricated for low IDDQ, signature analysis of IDDQ versus VDD can proceed apace for rapid identification of the root cause of defects and for improved corrective action. The measurement is simple [Fig. 2]. With the IC properly initialized and with its signal input pins set to appropriate logic states, VDD is varied while IDDQ is measured. An IC without defects usually has a flat, low nanoampere current signature. Figure 3 shows results for defects in microcontroller ICs. IDDQ signatures identify virtually instantaneously the probable category of defect.

The threat to IDDQ

What is the challenge to IDDQ testing posed by deep-submicron transistors? In a CMOS IC quiescent state, about half of the transistors are turned off, and each one in the off-state contributes a small, but important, leakage current (I_{off}) due mainly to junction leakage. When an IC has millions of transistors, then the total IDDQ (which is the sum of all transistor I_{off} leakages) will grow. The increase in transistor count, and associated total junction leakage, however, is by itself a relatively small factor compared with other mechanisms that add to I_{off} and IDDQ. The primary cause of heightened off-state leakage is a lowering in transistor threshold voltage (V_T).
Figure 4 illustrates an Ioff increase in a "long-channel" transistor. So what has $V_T$ to do with short-channel transistors? The answer lies in the lower $V_T$ values required by short-channel transistors. Deep-submicron transistor technologies are being forced to shift to lower power-supply voltages, VDD, to shrink the internal electric fields in the transistors and also to shrink power consumption. If dimensions are reduced for a fixed voltage, then internal electric fields will rise, increasing the reliability risk. Transistor threshold voltages are typically 0.7-1.0 V for 5-V technologies, where $V_T$ is about 15-20 percent of VDD. As VDD drops to the 1-2-V range, $V_T$ is projected to be reduced to about 0.3 V. If $V_T$ is not reduced as VDD drops, the high switching speed of the transistor suffers. As a result, Ioff and therefore IDDQ could subsequently rise from a few nanoamperes to tens of milliamperes or more, decreasing the effectiveness of IDDQ testing.

Other deep-submicron threats

In addition to lowered threshold voltage and many more transistors on the IC, several other mechanisms peculiar to deep-submicron transistors can bloat Ioff. Figure 5 illustrates the charge distribution of an n-channel transistor and one of the off-state leakage mechanisms that comes into being when the device is biased just below the threshold voltage.

Several off-state leakage current mechanisms exist at the deep-submicron level. They are collectively referred to as short-channel effects [Fig. 6].

I1 is the weak inversion current, which is negligible for long-channel transistors with their high threshold voltages, but can be the dominant leakage mechanism for short-channel transistors with low $V_T$. The weak inversion regions of the curves of Fig. 4 are their almost vertical portions.

I2 is the reverse-bias saturation current of a pn junction that occurs in drain-to-substrate and well-to-substrate regions. It is the dominant IDDQ leakage mechanism in ICs with long-channel transistors.

I3 is called the drain-induced barrier-lowering (DIBL) current. It is the channel surface current induced by the lowering of $V_T$.

I4 is an off-state leakage occurring deep in the channel and is called punchthrough. It starts when the charge-depletion regions of the drain and source respond to applied voltages by widening too much, to the extent that they "touch" and create a short between them. I3 and I4 are grim reminders of a basic transistor requirement: that the sum of the widths of the drain and source depletion regions must be kept smaller than the channel length.

I5 occurs when a full VDD bias voltage across the gate and drain terminals produces a large electric field at the oxide-to-drain interface. This intense field allows charge tunneling and the subsequent formation of hole-electron pairs from the kinetic energy of the tunneled charge. This leakage current is referred to as gate-induced drain leakage (GIDL). I6 represents tunneling of electrons across very thin gate oxides, and I7 is a current induced in trench-isolated technologies when the gate width becomes too narrow. The electric fields around the narrow gate structures are modified such that $V_T$ decreases with width and I7 increases. Whereas long-channel transistors had basically one off-state leakage mechanism, deep-submicron transistors may have as many as seven.

What can be done?

The challenge is obvious. IDDQ must be kept small despite the low threshold
voltages and short-channel current leakage mechanisms of submicron ICs. Short-channel effects have been controlled for channel lengths of 0.5-µm transistor ICs, but IDDQ increases into the tens of microamperes range have been measured for 0.35-µm ICs.

Processing techniques can help. To suppress the widths of the channel source and drain depletion regions, doping atoms are implanted at angles to the transistor surface. Thanks to these angled ion-implant paths, the placement of dopant ions can be more selective in the depletion region areas and the placement of doping atoms in the main portion of the channel can be discouraged. This doping profile reduces drain and source depletion-region widths, suppressing punchthrough and DIBL currents. When drain and source junctions are shallow, they provide better control of $V_T$ since there are fewer positive charges in these regions to horizontally image negative charges from the channel. Junctions as shallow as 10-20 nm have been reported for test transistors with channel lengths of 0.05-0.1-µm. Another proposed solution uses drain and source junctions that are recessed, with the gate region protruding slightly into the channel.

When transistor oxides are thinner, the gate voltage has more control of channel charges and short-channel effects are then suppressed. Oxides in the 1.5-6-nm range have been made for transistors on test chips.

Channel doping engineering is a key factor in reducing off-state leakage. Deep-submicron technologies will inherently have increased Ioff unless process engineers make strong efforts to control it.

**Technology tricks**

While process techniques and channel-drain engineering can keep the increases of Ioff to a minimum for short-channel transistors, what can test and product engineers do to control weak inversion current in the face of low threshold voltages and short-channel effects? Several possibilities exist.

One interesting technique takes advantage of the temperature properties of the weak inversion current. Charges move across the channel in the weak inversion state by diffusion whose rate is reduced as temperature is lowered. A calculation using weak inversion model equations showed that Ioff can be reduced by three to four orders of magnitude for $V_T = 0.3 \text{ V}$ if the measurement temperature is reduced from $22^\circ \text{C}$ to $-55^\circ \text{C}$. Any technique that reduces IDDQ by a factor of $10^4$ will enable IDDQ measurements useful for the ICs projected by the SIA Roadmap. Normal IDDQ values of 1-100 mA then shrink to 100 nA-10 µA for the IDDQ test.

Another approach, studied by researcher Manoj Sachdev, of Philips Laboratories, Eindhoven, the Netherlands, is to increase $V_T$ temporarily by increasing the source-to-substrate bias voltage. Back-bias substrate techniques were common practice for n-channel MOS technologies, but are more difficult for CMOS circuits. CMOS requires that substrates, wells, and source connections be electrically separable during IDDQ measurements, but have low ohmic connections during normal operation.

Sachdev has proposed a design in which all sources, wells, and substrate regions are connected to separate package pins. During the IDDQ measurement, the substrate and well back-biases would be driven at the pin level. IDDQ reductions on the order of $10^4$ are feasible, to judge by test chip transistor measurements. In fact, back-bias voltages can be driven to the limits of pn junction breakdown.

Built-in current sensors (BICSs) are another technological approach to the IDDQ testing of ICs with deep-submicron transistors. The concept involves building special sensors and test circuitry right into the IC structure. On command from control lines, the sensors measure IDDQ for a subcircuit of the IC. The idea is to have a built-in current sensor for a specific number of subcircuit transistors, no matter how large the circuit; the larger the circuit, the more BICSs. Experimental circuits and sensors have been put on test chips, but the concept needs to be tested more extensively before its long-term value can be assessed.

Another suggestion is to use transistors with different thresholds on the same IC. Transistors that are not critical to the speed of the IC are doped for higher thresholds, thus lowering their Ioff. A final suggestion involves the addition of more independent VDD pins. While efficient for separating the
noisier input and output buffer circuits from core logic, this approach does not offer the four-order-of-magnitude reduction in IDDQ required for the SIA Roadmap ICs.

To probe further

The National Technology Roadmap for Semiconductors (Semiconductor Industry Association, San Jose, Calif., 1994) may be obtained from Sematech Inc., 2706 Montopolis Dr., Austin, TX 78741; 512-356-3500.

Recommended conference Proceedings include those from the International Test Conference (ITC), International Electron Devices Meeting (IEDM), Custom Integrated Circuits Conference (CICC), and the Symposium on VLSI Technology.


The December 1992 issue of the Journal of Electronic Test: Theory and Applications (JETTA) is devoted to the subject of IDDQ testing.


About the authors

Jerry M. Soden is a senior member of the technical staff at Sandia National Laboratories, Albuquerque, N.M., in the failure analysis department. Since 1976, his responsibilities have included IC failure analysis, reliability testing, and design for reliability and testability. His research activities include IDQ testing, defect modeling, and the development of failure-analysis techniques for CMOS integrated circuits. Soden is a member of the program committee of the International Test Conference.

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